The microprocessor is an 80C31 with 8K of program memory (D27C64), 128 bytes of RAM, two counters, 32 I/O and boolean processing capabilities. The EP310 PLA provides Chip Select lines to the various peripherals.

Two peripheral interfaces (81C55 & 82C55) provide extra RAM, and an additional 46 I/O lines. These are used for real time clock control, SID/APL-2X1 control, front panel control, front panel switch inputs, reading the TDM shift register, non-volatile memory control, PLA control and analog control.

The RTC is a single chip (MM58174) time of day clock, with: month, day, hours, minutes, seconds, tenths. A uP software routine regularly interrogates the RTC and at 04:44:44.0 each day jams that value into a software counter. This routine keeps time referenced to input video in a drop frame mode. The RTC has its own 32768 Xtal and lithium battery backup. The quad analog switch (CD4066) is used to insure that the clock control lines are not disturbed during power interruptions.

The clock can be set via an RS-232C serial command, by a Front Panel "SET ?" command or by the auto set mode. (see the Operation section.)

The non-volatile memory is a 16 bit by 16 word serial EEPROM. Control is via PA.3-.0 of the 81C55. The memory is used to store the data which is inserted into the SID signal, the source number, and the status bits. The memory is read on power up, and after a store command (XFR DATA).

The front panel display is an eight character alpha-numeric LED type (PD2816). The 64 character ASCII font can be shown. The type of display shown is selected by pressing the front panel pusbuttons (see the Operation section).

The front panel aslo contains the four DIP switches and six operation pushbuttons. The data to and from the front panel is in a serial format. Two serial-to-parallel shift registers (HC164) provide access to the display. Two parallel-to-serial shift registers provide access to switches. The front panel is read and written to once each field. Software routines perform the debounce functions for the switches.

The master clock for the SGR is a 512xH (8.055MHz) crystal controlled oscillator (HCU04). This provides the clock for the uP, SYNCGEN PLA (EP600), the SID/TDM shift register control PLA, and the internal (80C31) counters.

The 8.055HMz clock is divided by two in the EP310, and fed to the SyncGen PLA, if input video is absent. The SyncGen PLA generates a composite sync signal which is fed to the SID/SYNC summing amplifier (LM318). When input video is removed, a different monitor program is invoked by the processor to control the SyncGen PLA. The SID/APL-2X1 is switched to the SID & SYNC side, and the PGM-2X1 is switched to the SID/APL input. The Horizontal Drive one-shot is now triggered from the PLA output. This forces the PLL to reference to the SyncGen signal. The resultant video signal produced is black (no burst or setup) with SID information. In addition, the Exciter output is forced to a high state. Therefore, even if program video is lost, the transponder will always see a video signal.

The power supplies are linear full wave center tapped transformers. The +/- 8 volt rails are powered by monolithic regulators (7808, 7908). The +5V supply is slightly more complicated. The LM2935 regulator provides a constant low current output, which is used to control the power-up sequence (LM393) of the main +5, and the power-on-reset pulse to the uP (LM393). When power is first applied, the reset line will be high, and the main +5V will be zero volts. After about 500mS, the main +5V power will be enabled, and about 100mS later the reset line will go low, which will enable the processor to begin execution of the program. Any minor interruption in power will result in the activation of the 600mS power-on-sequence and reset circuits.

Timing: items are referenced to the 64H 1.00699MHz clock one count=993nS

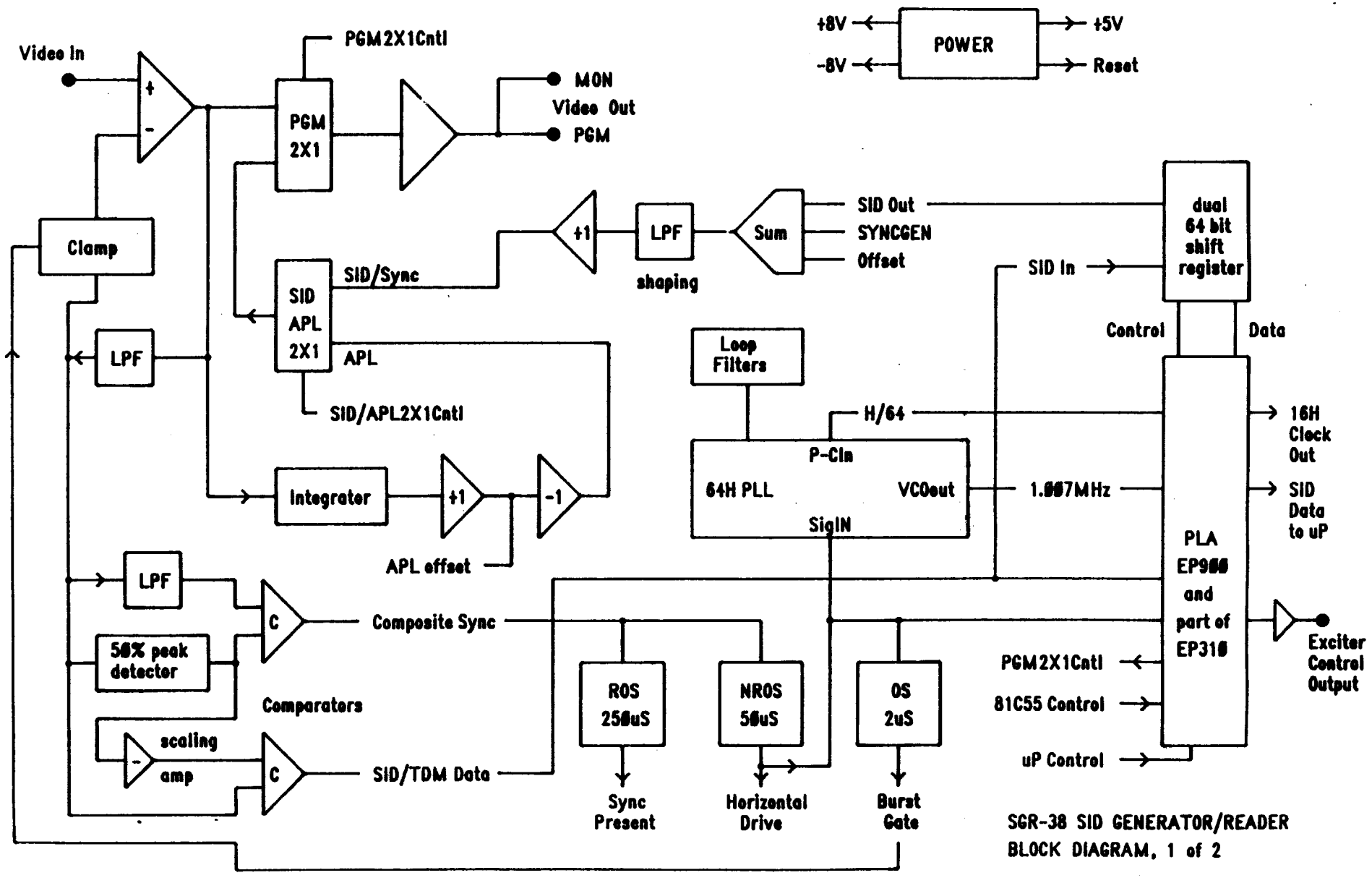
SID output: the SID output will begin at the 12th count of the 64H clock, measured from the leading edge of input sync. The output level will be 50 +10, -0 IRE, jitter less than 100nS.

TDM input: the TDM data word should begin at the 16th count of the 64H clock, with each bit period being 4 counts in duration (3.97uS). The end of the signal will then be at the 48th count. The input level should be 50 +/- 5 IRE.

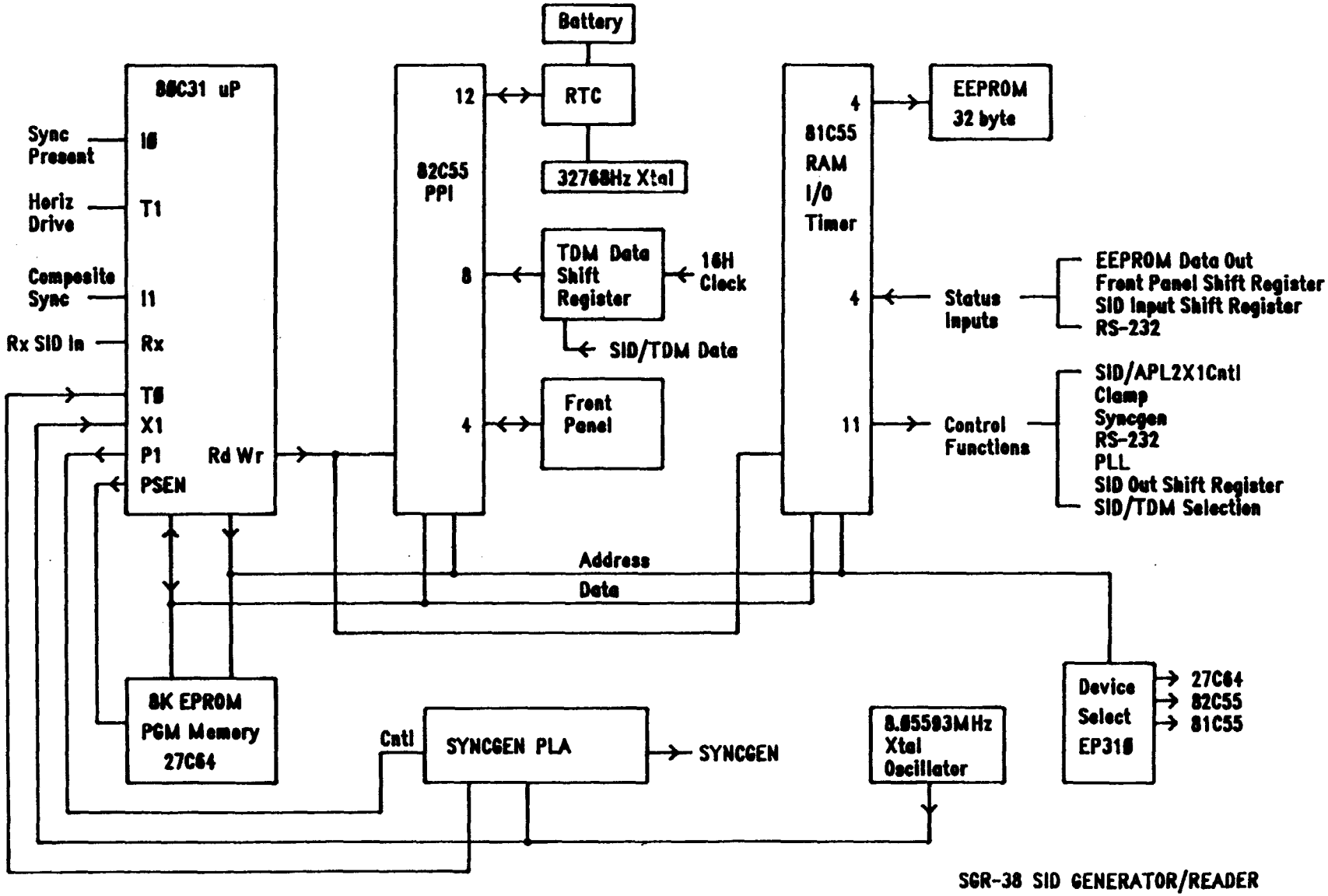
Exciter: the Exciter switch will occur at the 22nd count of the 64H clock on line 15. The output level is a standard LSTTL drive, Voh=2.4Vmin. Switch point variation will be +/- 100nS.

Black: When input video is removed, the unit will enable the sync generator PLA and produce black video with SID. The 64H PLL will now lock to the SYNCGEN output. The video will include normal H sync, and vertical sync with equalizing and serration pulses, in an interlaced format.

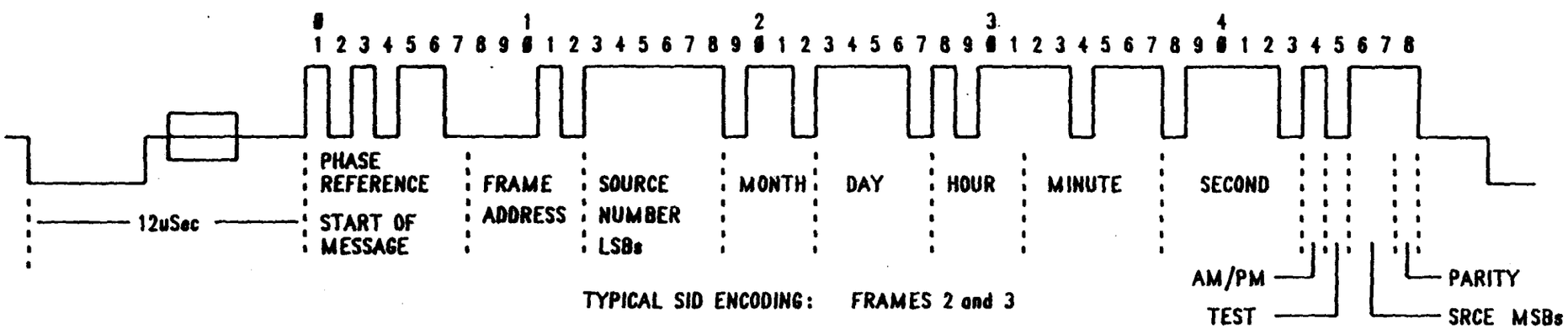
APL: When in the TDM mode, the SGR will maintain a constant APL signal to the exciter input. Variation will be +/-3IRE.



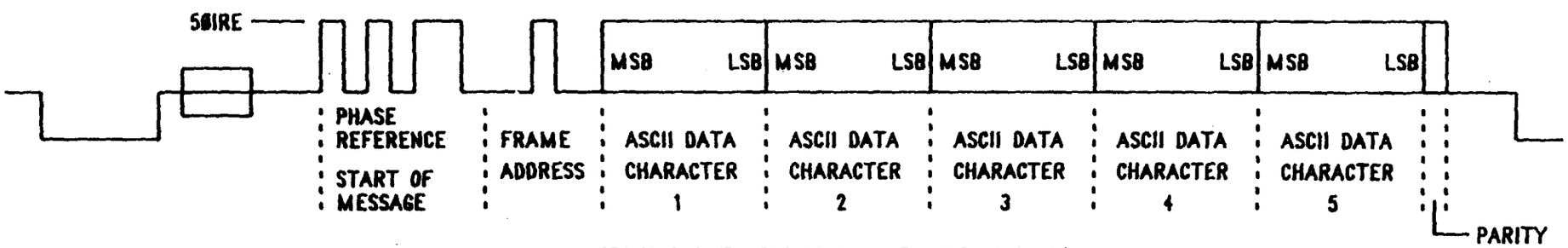
SGR-38 SID GENERATOR/READER
BLOCK DIAGRAM, 1 of 2



SGR-38 SID GENERATOR/READER
BLOCK DIAGRAM, 2 of 2

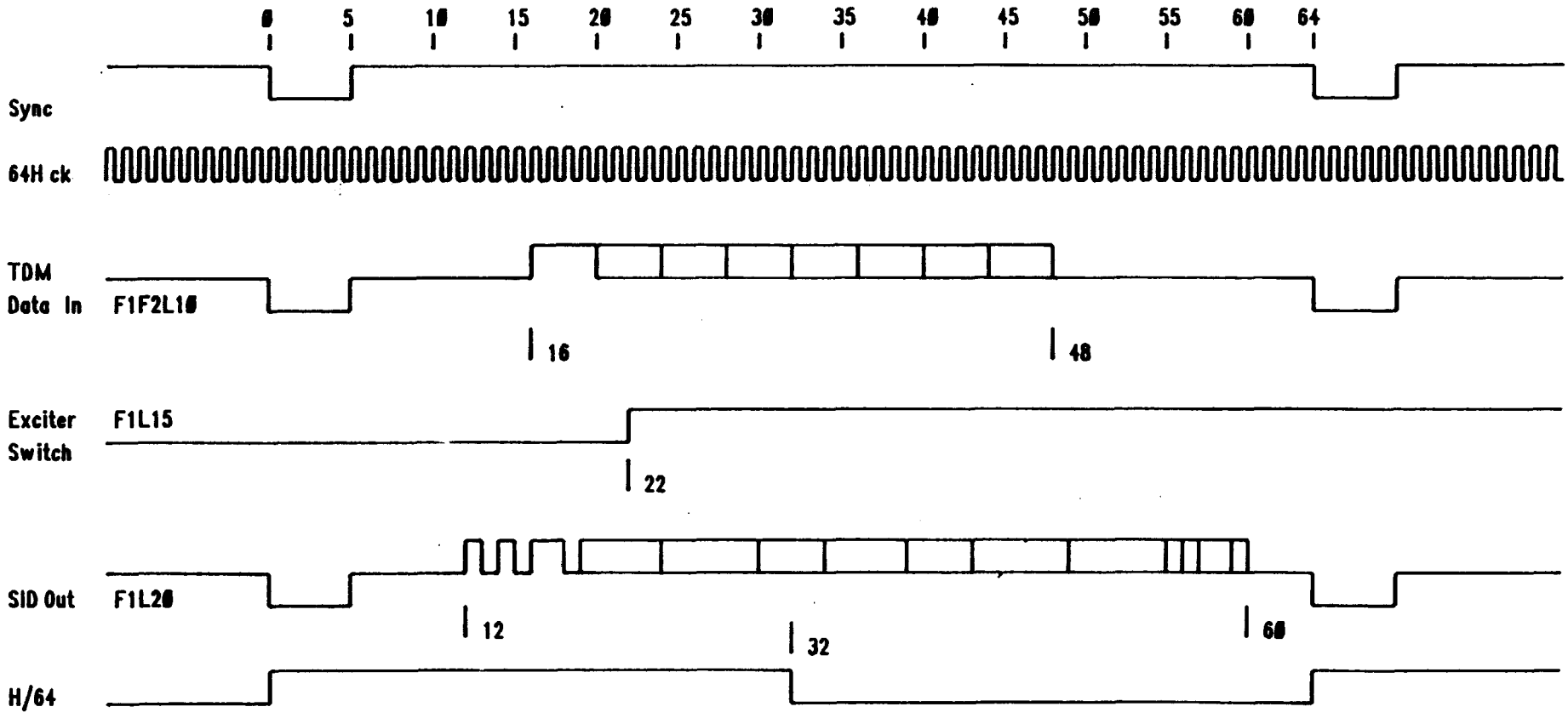


TYPICAL SID ENCODING: FRAMES 2 and 3



TYPICAL DATA ENCODING: FRAMES 4 to 15

SGR-38 SID GENERATOR/READER
ENCODING FORMAT, FIELD ONE, LINE 20



SGR-38 SID GENERATOR/READER
PLL TIMING